Research on the Buck Converter's Efficiency

Bachelor Thesis by

Manuel Ayuso de Francisco

Blekinge Institute of Technology

School of Engineering

Department of Electrical Engineering

Supervisor: Anders Hultgren

Examinar: Sven Johansson

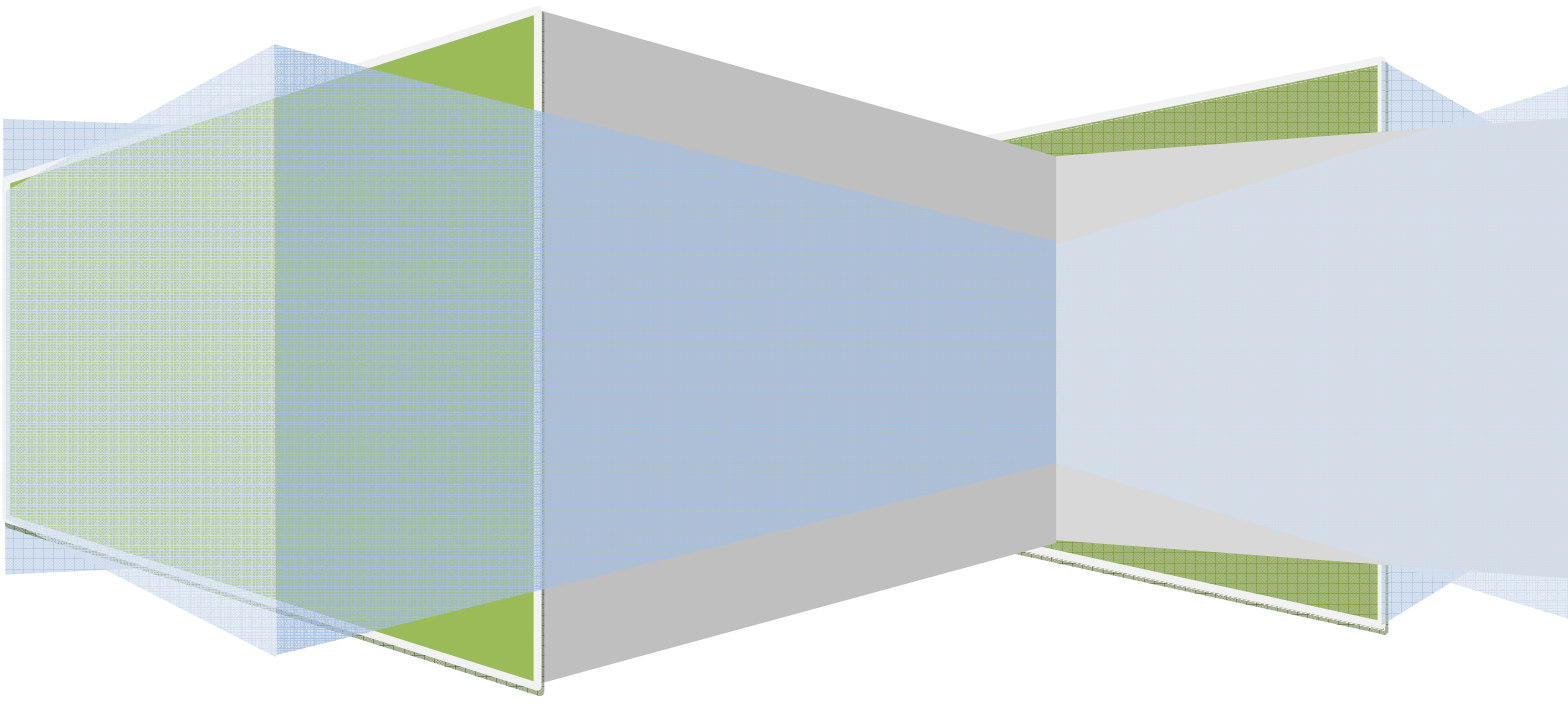


Table of Contents

List of Figures

List of tables

Acknowledgment

A short paragraph is never enough to express the gratitude to all those who have been part of me during this time.

I still remember my first day in Karlskrona. It was the sixteenth of August and I was here, alone, trying to be accepted at the BTH, but my whish of doing the bachelor thesis in Sweden seemed almost impossible. But then something happened, my coordinator, Lina Berglind called Anders Hultgren, who in less than one minute was totally disposed to be my supervisor. Therefore, he is not only my supervisor but also the reason why I am here. So, I want to express my sincere gratitude to Anders Hultgren, for his knowledge and mainly for being such a close person.

To all my big family, Jose, Dani, Iker, Max, Amaia, Vanesa, Eva, Fer, Antonio, Sandra, Sara, Loreto, Cloi and many other persons who have disturbed me during my hours of study, because without all those disturbances, this thesis would never have come true.

To Jacopo, because he has always offered me his patience and has been the real motivation and support that I needed.

To Samu, of course.

1. Introduction:

Over the last decades, the use of electronic devices has become an essential part in our daily lives. The development on this area is closely related to reduce as much as possible the size of these devices, being the power consumption the limiting factor when the aim is to get a high efficiency.

1.1 Thesis Background:

Nowadays, almost every kind of electronic devices are portable and therefore powered by battery. That battery provides a constant voltage; hence a voltage regulator is increasingly necessary. A voltage regulator is an electronic device which provides a constant output voltage, regardless of the input voltage. Also, the input current can be regulated or unregulated. These devices are commonly known as DC/DC Converters. As the performance increased in circuitry, other more efficient DC converters were needed. That requirement promoted a way of designing based on computerizing the control of power converters [13 and 14]. The most frequently used power converters are DC/DC Converters of Buck type.

At the present, every electronic component is powered by a DC source. Usually, this requires the previous conversion of current. We can find three types of power conversion devices:

1. AC/DC: Most known as power supply in which alternating current becomes direct.
2. DC/DC: Converters. It supposes a change of DC values.
3. DC/AC: Act as inverter.

1.2 Objectives:

The main target of this project is to work on an alternative design of the buck converter, focusing the topic on a deep study of the efficiency. Therefore, apart from the mathematical design, chapter 4 and 5 are all about the choice of the appropriate components and its behavior in the Buck Converter.

1.3 Outline of the Thesis:

Apart from this first introductory chapter, the second chapter provides a general vision about the buck converter, consisted on its different topologies, basics of the system and modes of operation. The third chapter is about the mathematical analysis of the converter. The choice of the components is tackled in chapter four, while the efficiency of the system based on the components behavior is studied in chapter five. The results of the simulation are shown in chapter six and also parallel experiments changing different values to test the efficiency. To sum up, chapter seven tells about the conclusions and chapter eight provides all the references used in this thesis work.

2. The Buck Converter:

A SMPS (switched-mode power supply) is a nonlinear power converter which holds a high efficiency rate. The most common SMPS is the Buck Converter, in which the output voltage is always lower than the input. A SMPS is a circuit in which AC is rectified and converted into DC unregulated. It means that the DC produced may have fluctuations due to variations in the main supply. To produce regulated output dc voltage it is necessary to set a feedback control circuit to sense the output voltage and adjust the power transfer in order to produce a constant output. [1, 2, 3, 13 and 14]

2.1. Typologies:

This kind of converter is used in order to generate a different output voltage below the input voltage. This topology is based on a circuit with a single- and two-switch implementation shown in the next figure.

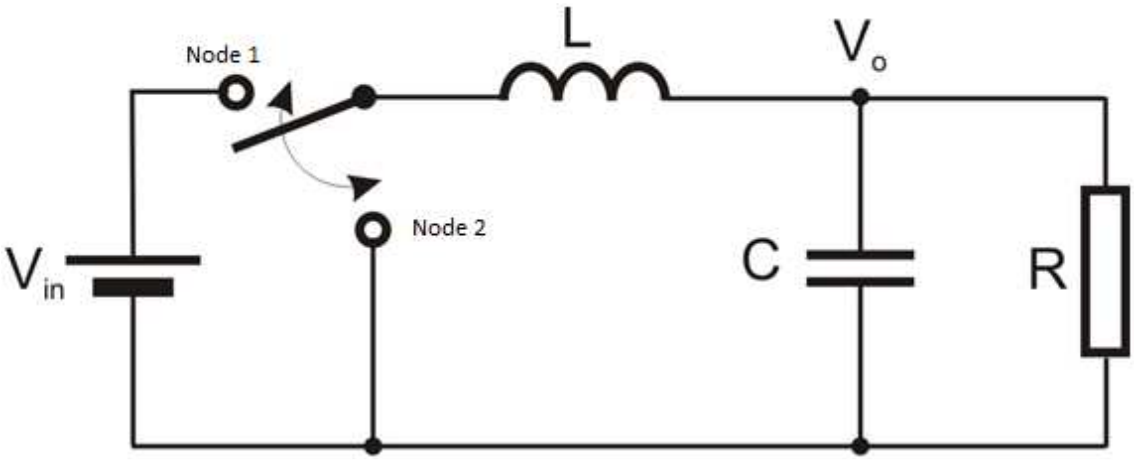


Figure 1. Single-pole, double-throw switch implementation.

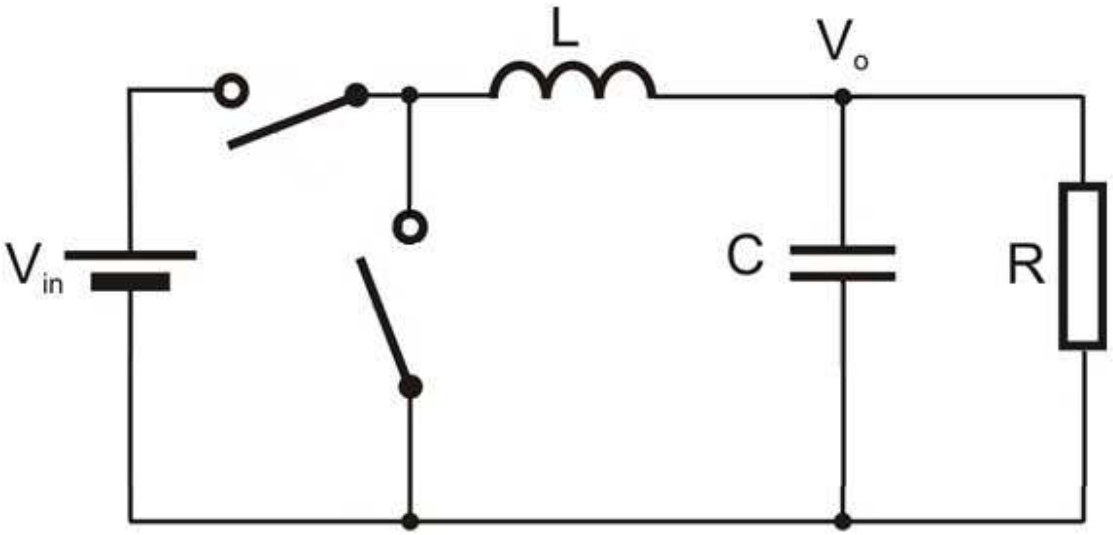


Figure 2. Two-switch implementation.

Also, it can be implemented using a transistor and a diode:

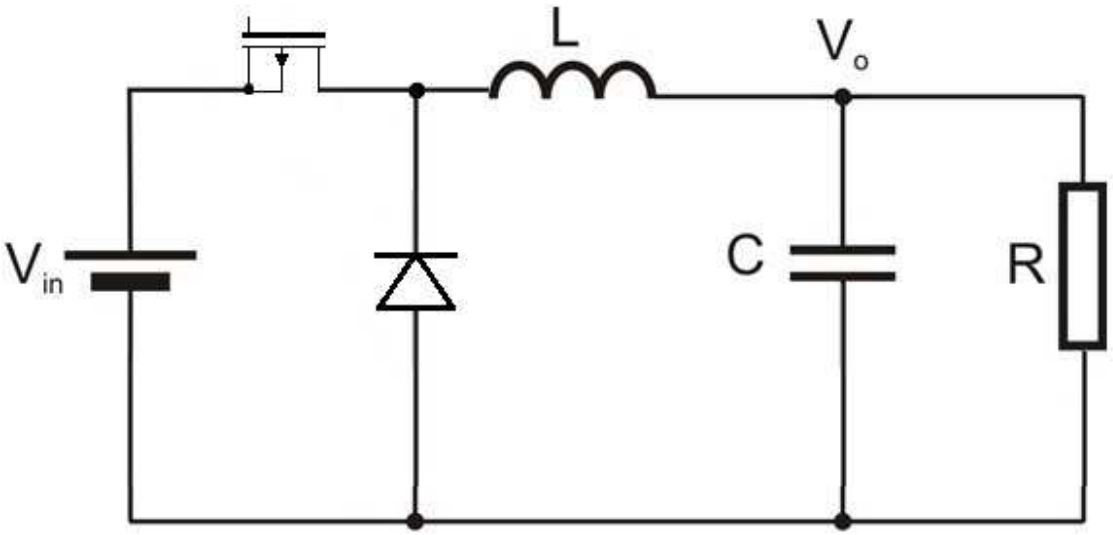


Figure 3. Mosfet and diode implementation.

As we said before the buck converter is a non linear system, so there are some impedances due to the capacitor and inductor, so the real circuit would be the next one:

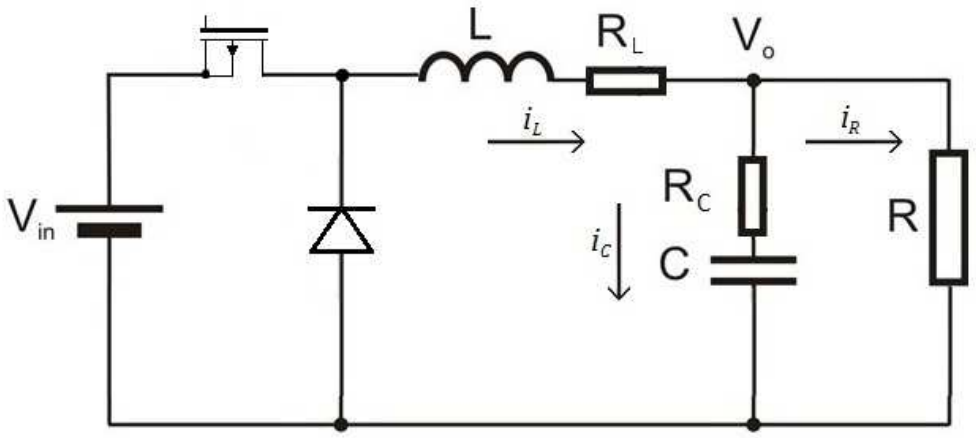


Figure 4. Nonideal Buck Converter.

2.2. Basics of the system:

The output voltage produced V_0 consists of the desired dc and the undesired ac components. Practically, the output ripple due to switching is very small compared to the level of the dc output voltage.

Considering lossless components and ideal switching devices, the two different average power, input power and output power are equal[1]:

$$Pin = Po \tag{2.1}$$

Since the inductor current and the capacitor voltage are periodic over one switching cycle:

$$i_L(t_0) = i_L(t_0 + T) \tag{2.2}$$

$$v_c(t_0) = v_c(t_0 + T) \tag{2.3}$$

Since capacitors and inductors are ideal, the average inductor voltage and the average capacitor current are zero:

$$I_c = \frac{1}{T}\int_{t_0}^{T+t_0} i_c(t)\,dt = 0 \tag{2.4}$$

$$V_L = \frac{1}{T}\int_{t_0}^{T+t_0} v_l(t)\,dt = 0 \tag{2.5}$$

These two equations suggest that the total energy stored in capacitor and inductor over one period of time is zero. So finally the switching waveform for the power switch is the one given in the next figure[2]:

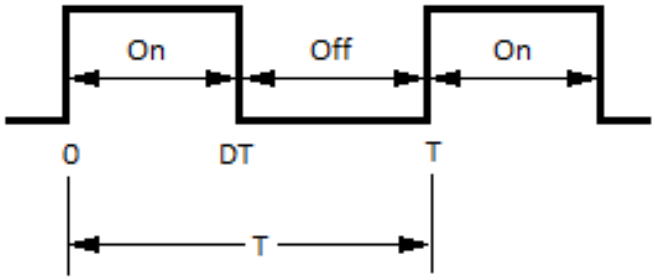


Figure 5. Switching waveform for the power switch

2.3. Operation. The Duty cycle and PWM:

2.3.1. The Duty Cycle:

The term duty cycle referees to the proportion of ON time compared to the full time [3]. In other words, the proportion of time in which voltage is supplied to the circuit.

$$D = \frac{\tau}{T} \tag{2.6}$$

D Duty cycle.

τ ON time.

T Function period.

When the switch is OFF there is not current, however when it is ON, all the current is supplied.

If we assume D as the duty cycle defined in this equation: $D = ton/T$ then the power transistor is turned on for a period of DT and turned off for the remaining time $(1 - D)T$.

2.3.1.1 PWM. Variable duty cycle system:

Firstly, this current is supplied to the switching section of the buck converter with high frequency, which switches energy pulses with variable duty cycle and constant voltage magnitude to the system. Secondly, these energy pulses are filtered by a low pass filter (inductor and capacitor) providing a low tension ripple across the capacitor. The input voltage

supplied to the LC circuit is controlled by a PWM (pulse width modulation). PWM is a technique used for controlling power to internal electrical devices. It works modifying the duty cycle to get the minimal power loss, keeping the frequency of operation constant [13]. The frequency of the PWM must be higher than the LC filter frequency.

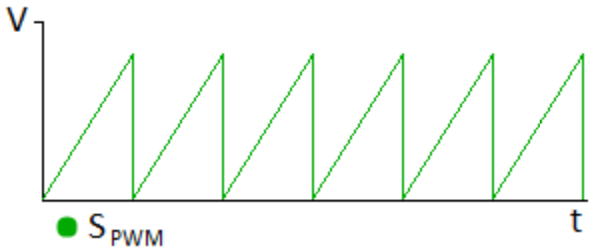


Figure 6. PWM signal.

To modify the duty cycle, the output voltage is fed back and dicretized to be compared to the PWM. To dicretize it, we will divide the output voltage by V_G, creating a new parameter D. When D is bigger than the PWM signal the switch is connected to node 1, which keeps the source connected to the circuit, otherwise the switch is connected to node 2 and the input voltage will be 0V. As a result PWM provides a great method to reach a high efficiency.

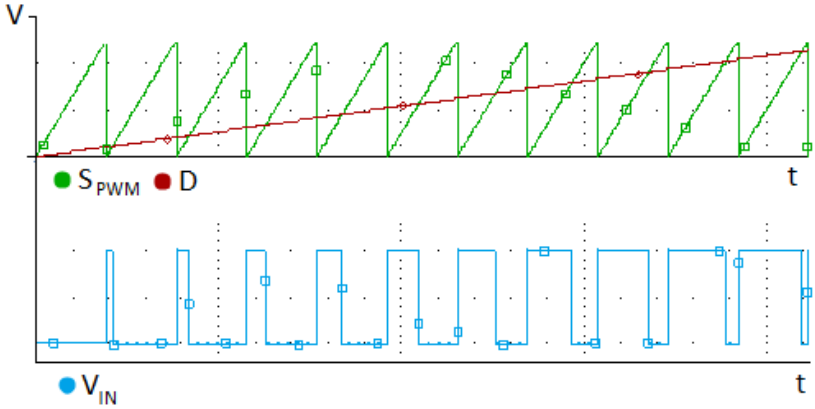


Figure 7. Comparison between PWM signal and feedback signal.

2.3.1.2 PWM. Constant duty cycle system:

Since the task of this project is to choose the most proper elements which provide us the highest efficiency, the feedback topic does not concern us. Also the duty cycle can be set to a constant value.

2.4 Modes of operation:

Depending on which node is the system connected there are two different states of operation, ON State and OFF State [1,2 and 3].

2.4.1. ON State:

The energy transferred comes directly from the source to the inductor and so current across the inductor increases progressively.

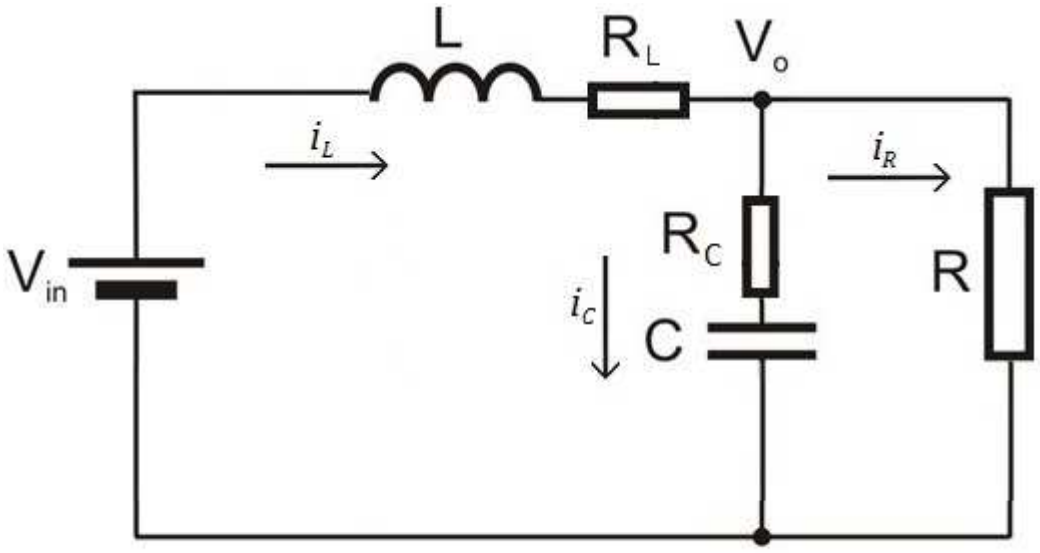


Figure 8. Switched connected to node one. ON State.

2.4.2. OFF State:

When the switch is connected to node two the inductor acts as a source supplying the energy stored to the load. In this case, the current through the circuit decreases according to the inductor's discharge.

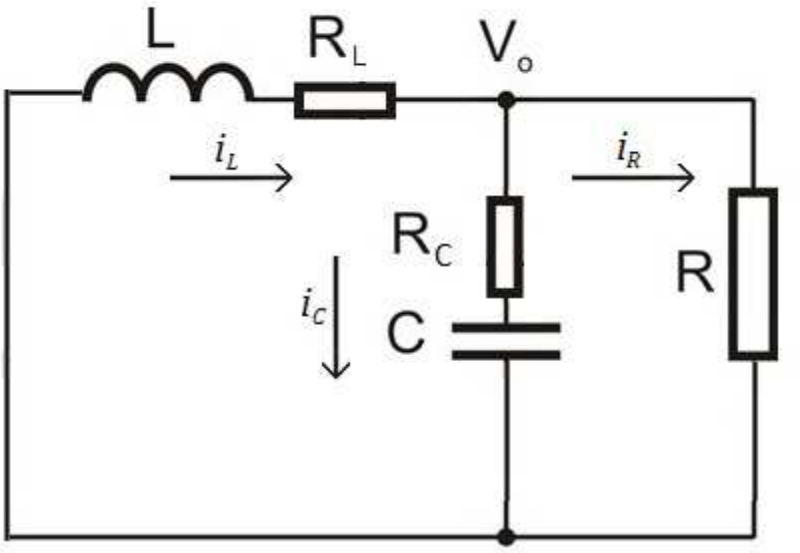


Figure 9. Switched connected to node two. OFF State.

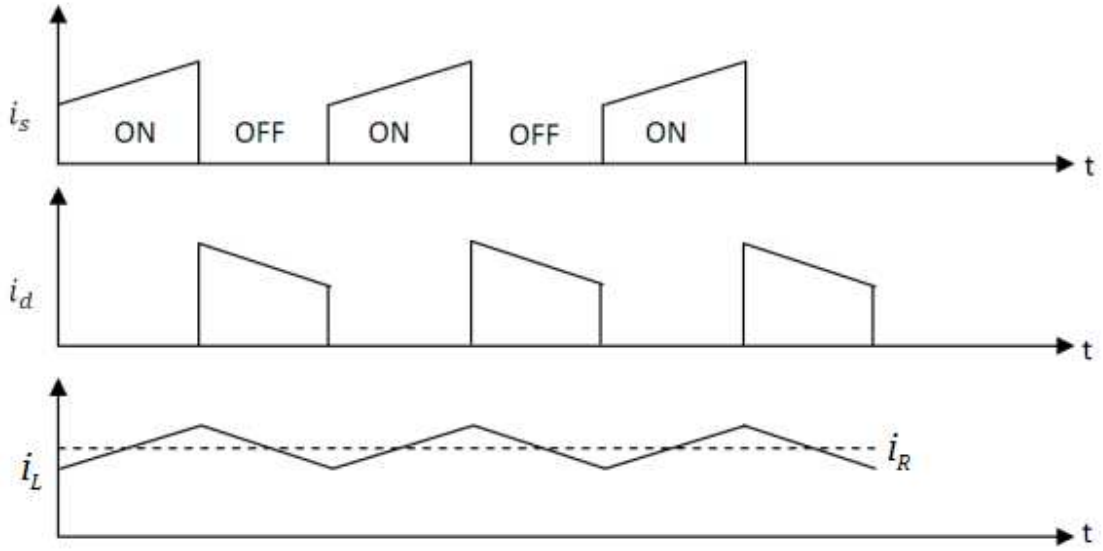


Figure 10. The different currents during the two states of operation. First the current is supplied by the source and secondly by the inductor [14].

3. Mathematical Modeling of a Buck Converter:

3.1 Space state equations:

To describe the system we will use differential equations which explain the different relations between the components of the circuit. The state vector $x(t)$ is composed by capacitor voltages and inductor currents. $u(t)$ is a input vector formed by grouping the sources. The output vector $y(t)$ is dependent on the two vectors mentioned before, $x(t)$ and $u(t)$.

$$K\frac{dx(t)}{dt} = Ax(t) + Bu(t) \quad (3.1)$$

$$y(t) = \mathrm{C}x(t) \quad (3.2)$$

The term K groups the values of capacitors and inductors.

According to what was said before there are two states of operation so it can be possible that the different matrix might change in each state. As a result, the analysis will be specific for each mode. The first, including the source V_g for a d time and the second without the source for a $d' = (1 - d)$ time.

$$A = dA_1 + d'A_2 \quad (3.3)$$

$$B = dB_1 + d'B_2 \quad (3.4)$$

$$C = dC_1 + d'C_2 \quad (3.5)$$

3.1.1. Model with voltage source:

The switch is connected to node one, so the system is set to ON State.

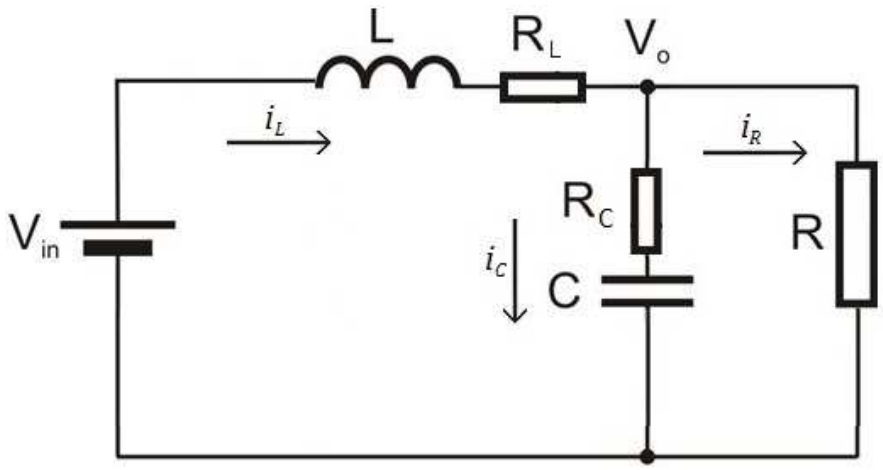


Figure 11. Model with voltage source.

Using Kirchhoff Voltage and Current laws the analysis of the circuit is the next.

$$-V_g + R_L i_L + L\frac{di_L}{dt} + V_0 = 0$$

$$L\frac{di_L}{dt} = V_g - R_L i_L - V_0 \quad (3.6)$$

$$i_C = i_L - i_R \quad (3.7)$$

According to Ohm's law:

$$i_C = i_L - \frac{V_0}{R} \quad (3.8)$$

And

$$V_0 = V_C + i_C R_C \quad (3.9)$$

So

$$i_C = \frac{V_0 - V_C}{R_C} \quad (3.10)$$

if we equate equation 3.8 and 3.10 we get

$$i_L - \frac{V_0}{R} = \frac{V_0 - V_C}{R_C} \quad (3.11)$$

Solving V_0 from the equation written before:

$$V_0 = \frac{R.R_C}{R+R_C}\left(i_L + \frac{V_C}{R_C}\right) \quad (3.12)$$

If we substitute equation 3.12 in equation 3.10:

$$i_C = \frac{\frac{R.R_C}{R+R_C}\left(i_L + \frac{V_C}{R_C}\right) - V_C}{R_C}$$

$$i_C = \frac{\frac{R.R_C}{R+R_C} i_L + V_C \frac{R}{R+R_C} - V_C}{R_C}$$

$$i_C = \frac{R}{R+R_C} i_L + V_C \frac{R.R_C}{R+R_C} - \frac{V_C}{R_C}$$

$$i_C = \frac{R}{R+R_C} i_L + V_C \left(\frac{R.R_C}{R+R_C} - \frac{1}{R_C}\right)$$

$$i_C = \frac{R}{R+R_C} i_L - \frac{V_C}{R+R_C} \tag{3.13}$$

Since we are looking for capacitor voltages:

$$C\frac{dV_C}{dt} = \frac{R}{R+R_C} i_L - \frac{V_C}{R+R_C} \tag{3.14}$$

From equation 3.6 and 3.12:

$$L\frac{di_L}{dt} = V_g - i_L\left(R_L + \frac{R.R_C}{R+R_C}\right) - \frac{R.V_C}{R+R_C} \tag{3.15}$$

Using equations 3.14 and 3.15 :

$$\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix} \begin{bmatrix} \frac{di_L}{dt} \\ \frac{dV_C}{dt} \end{bmatrix} = \begin{bmatrix} -\left(R_L + \frac{R.R_C}{R+R_C}\right) & -\frac{R}{R+R_C} \\ \frac{R}{R+R_C} & -\frac{1}{R+R_C} \end{bmatrix} \begin{bmatrix} i_L \\ V_C \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \end{bmatrix} V_g \tag{3.16}$$

$$\begin{bmatrix} V_0 \\ i_R \end{bmatrix} = \begin{bmatrix} \frac{R.R_C}{R+R_C} & \frac{R}{R+R_C} \\ \frac{R_C}{R+R_C} & \frac{1}{R+R_C} \end{bmatrix} \begin{bmatrix} i_L \\ V_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} V_g \tag{3.17}$$

$$A_1 = \begin{bmatrix} -\frac{1}{L}\left(R_L + \frac{R.R_C}{R+R_C}\right) & -\frac{1}{L}\frac{R}{R+R_C} \\ \frac{1}{C}\frac{R}{R+R_C} & -\frac{1}{C(R+R_C)} \end{bmatrix} \tag{3.18}$$

$$B_1 = \begin{bmatrix} 1 \\ 0 \end{bmatrix} \tag{3.19}$$

$$C_1 = \begin{bmatrix} \frac{R.R_C}{R+R_C} & \frac{R}{R+R_C} \\ \frac{R_C}{R+R_C} & \frac{1}{R+R_C} \end{bmatrix} \quad (3.20)$$

3.1.2. Model without voltage source

The switch is connected to node two, so the system is set to OFF State.

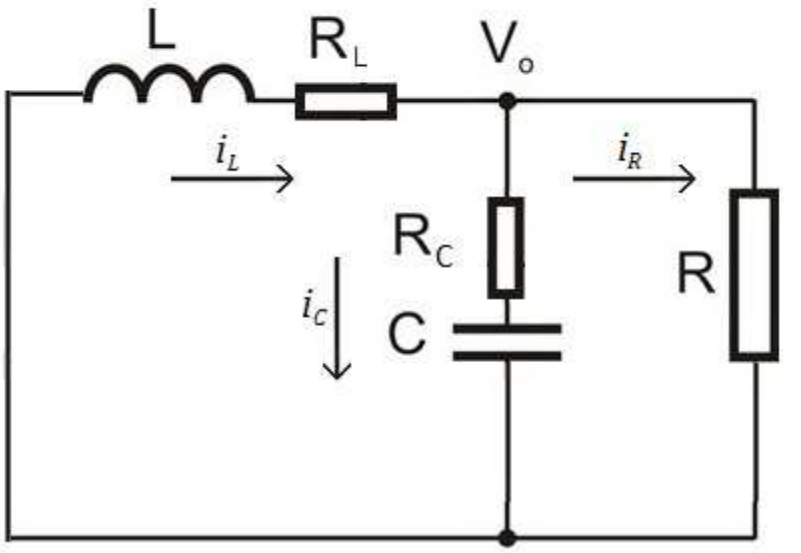


Figure 12. Model without voltage source.

Using Kirchhoff Voltage and Current laws the analysis of the circuit is the next.

$$R_L i_L + L\frac{di_L}{dt} + V_0 = 0$$

$$L\frac{di_L}{dt} = -R_L i_L - V_0 \quad (3.21)$$

$$i_C = i_L - i_R \quad (3.22)$$

According to Ohm's law:

$$i_C = i_L - \frac{V_0}{R} \quad (3.23)$$

And

$$V_0 = V_C + i_C R_C \tag{3.24}$$

So

$$i_C = \frac{V_0 - V_C}{R_C} \tag{3.25}$$

if we equate equation 3.23 and 3.25 we get

$$i_L - \frac{V_0}{R} = \frac{V_0 - V_C}{R_C} \tag{3.26}$$

Solving V_0 from the equation written before:

$$V_0 = \frac{R.R_C}{R+R_C}\left(i_L + \frac{V_C}{R_C}\right) \tag{3.27}$$

If we substitute equation 3.27 in equation 3.25:

$$i_C = \frac{\frac{R.R_C}{R+R_C}\left(i_L + \frac{V_C}{R_C}\right) - V_C}{R_C}$$

$$i_C = \frac{\frac{R.R_C}{R+R_C} i_L + V_C \frac{R}{R+R_C} - V_C}{R_C}$$

$$i_C = \frac{R}{R+R_C} i_L + V_C \frac{R.R_C}{R+R_C} - \frac{V_C}{R_C}$$

$$i_C = \frac{R}{R+R_C} i_L + V_C \left(\frac{R.R_C}{R+R_C} - \frac{1}{R_C}\right)$$

$$i_C = \frac{R}{R+R_C} i_L - \frac{V_C}{R+R_C} \tag{3.28}$$

Since we are looking for capacitor voltages:

$$C\frac{dV_C}{dt} = \frac{R}{R+R_C} i_L - \frac{V_C}{R+R_C} \tag{3.29}$$

From equation 3.21 and 3.27:

$$L\frac{di_L}{dt} = -i_L(R_L + \frac{R.R_C}{R+R_C}) - \frac{R.V_C}{R+R_C} \tag{3.30}$$

Using equations 3.29 and 3.30 :

$$\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix}\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dV_C}{dt} \end{bmatrix} = \begin{bmatrix} -(R_L + \frac{R.R_C}{R+R_C}) & -\frac{R}{R+R_C} \\ \frac{R}{R+R_C} & -\frac{1}{R+R_C} \end{bmatrix}\begin{bmatrix} i_L \\ V_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} V_g \tag{3.31}$$

$$\begin{bmatrix} V_0 \\ i_R \end{bmatrix} = \begin{bmatrix} \frac{R.R_C}{R+R_C} & \frac{R}{R+R_C} \\ \frac{R_C}{R+R_C} & \frac{1}{R+R_C} \end{bmatrix}\begin{bmatrix} i_L \\ V_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} V_g \tag{3.32}$$

$$A_2 = \begin{bmatrix} -\frac{1}{L}(R_L + \frac{R.R_C}{R+R_C}) & -\frac{1}{L}\frac{R}{R+R_C} \\ \frac{1}{C}\frac{R}{R+R_C} & -\frac{1}{C(R+R_C)} \end{bmatrix} \tag{3.33}$$

$$B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{3.34}$$

$$C_2 = \begin{bmatrix} \frac{R.R_C}{R+R_C} & \frac{R}{R+R_C} \\ \frac{R_C}{R+R_C} & \frac{1}{R+R_C} \end{bmatrix} \tag{3.35}$$

3.1.3 Average model:

For the average model we will use matrix A, B and C. After these calculations we observed that $A_1 = A_2$ and also $C_1 = C_2$.

- $K\frac{dx(t)}{dt} = (A_1 d + A_2(1-d))x(t) + (B_1 d + B_2(1-d))u(t)$

$$=((A_1 - A_2)d + A_2)\,x(t) + ((B_1 - B_2)d + B_2)\,u(t)$$

$$A_1\,x(t) + Bd \tag{3.36}$$

Since matrix

$$B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

So

$$B = B_1\,u(t)$$

- $y(t) = (C_1 d + C_2(1-d))x(t)$

$$=((C_1 - C_2)d + C_2)\, x(t)$$
$$= C_2 x(t) \qquad (3.37)$$

4. Components chosen for the design:

As it was said before, the behavior of the different components of the system is non-ideal so, to choose properly the different components, we have to specify which maximum range of looses is accepted.

Firstly, we will take into account some previous specifications. Nevertheless, some of them will be changed in the next paragraph:

$$I_{NOM} = 5A$$
$$V_0 = 5V$$
$$V_{NOM} = 5V$$
$$V_{IN} = 12V$$
$$\Delta I \leq 25\%$$
$$\Delta V_0 = 1\%$$

4.1. Inductor:

The main function of the inductor is to supply constant power to the resistance. It happens when the switch is OFF and no source is connected to the circuit. In that case, the power is supplied by the inductor, transferring current to the load. First, assume the converter is in continuous-current mode which implies that the inductor does not fully discharge during the switch-off time [14].

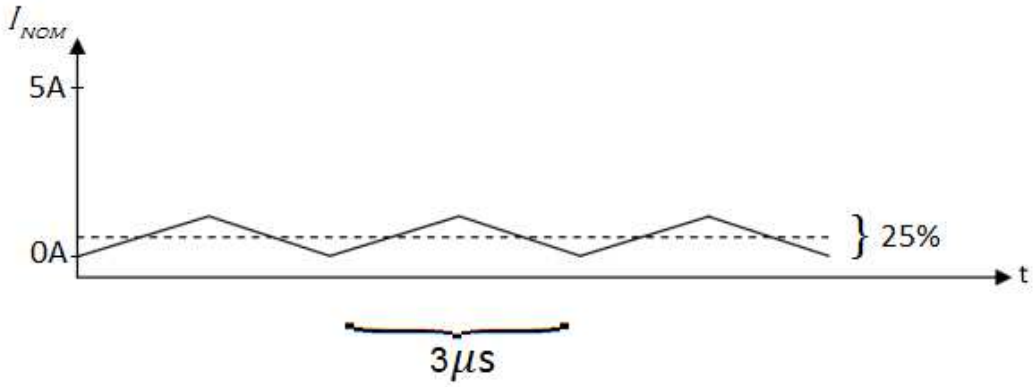


Figure 13. Inductor current.

If we analyze the voltage across the inductor during the ON period, then:

$$V_L = \frac{1}{T_{ON}} \int_0^{T_{ON}} v_l(t)\, dt = \frac{1}{T_{ON}} T_{ON}(V_G - V_0) =>$$
$$=> di_L = \frac{1}{L}(V_G - V_0)dt \quad (4.1)$$

And, for a short interval:

$$\Delta i_L = \frac{1}{L}(V_G - V_0)\Delta t => \ 0.25 * 5 = \frac{12-5}{L} 1.5\mu s$$
$$=> L = 8.4\mu H$$

Peak current through the inductor determines the inductor's required saturation-current rating. Saturating the inductor core decreases the converter efficiency, while increasing the temperatures of the inductor, the MOSFET and the diode.

The inductor's peak operating currents is calculated as follows:

$$I_{peak} = I_0 + \frac{I_0 \Delta I_0}{2} = 5.625A \quad (4.2)$$

We will make sure that the saturation-current rating is higher than the calculated peak current. In these conditions the inductor chosen is:

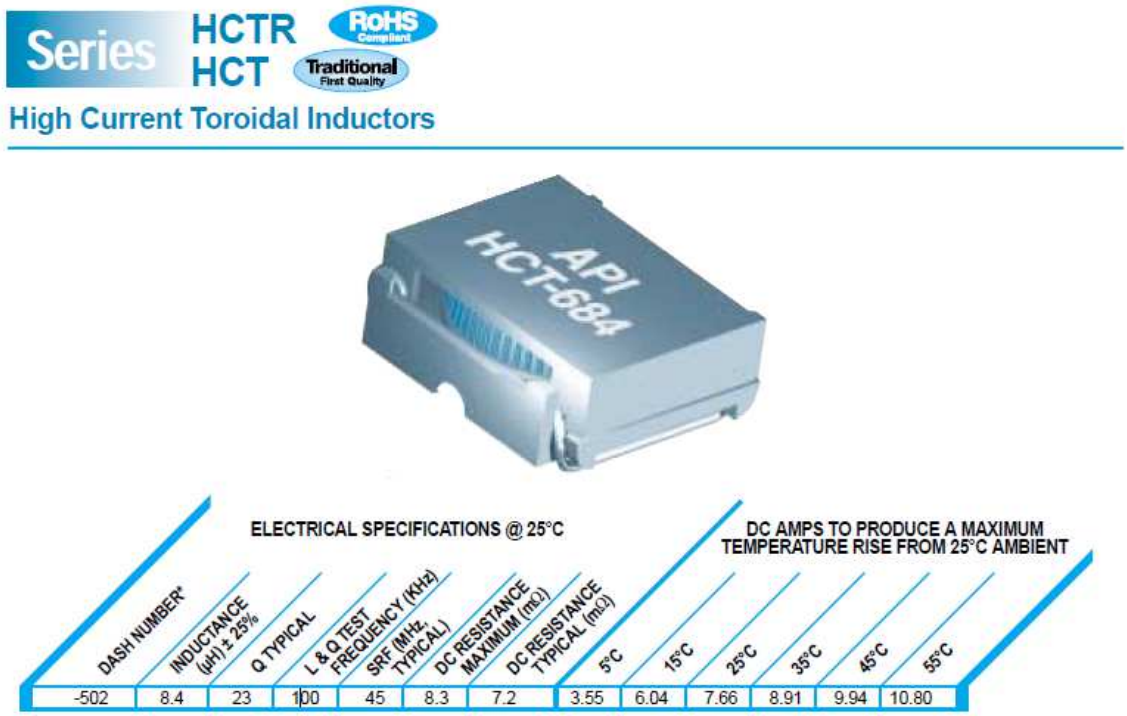


Figure 14. Inductor datasheet.

Where DC RESISTANCE MAXIMUM will be called from now on R_L.

4.2. Capacitor:

The capacitor is used to reduce voltage ripples and overshoots because acts as low pass filter. Large overshoots are caused by insufficient output capacitance, and large voltage ripple is caused by insufficient capacitance as well as a high ESR (equivalent-series resistance) in the capacitor. [4]

We cannot use a general value for the current across the capacitor so we will use the charge Q.

And according to this figure

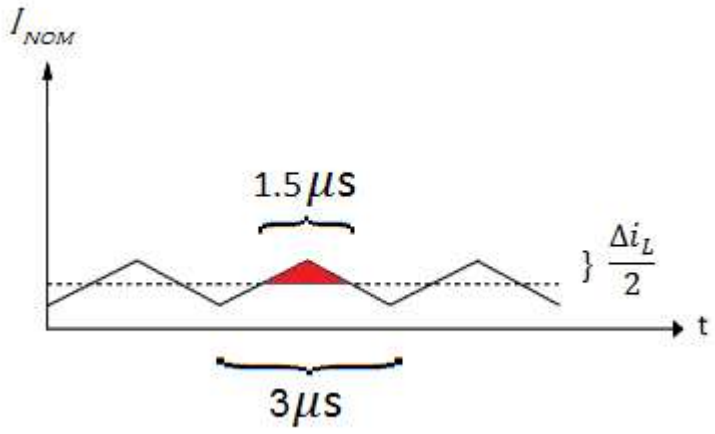


Figure 15. Charge stored by the capacitor.

We will use the area colored in red which will give us an average value of the charge stored by the capacitor.

We know that:

$$Q = \int i_C \, dt \tag{4.3}$$

Instead of using integrals we will calculate it by trigonometry that, in this case results really useful.

So:

$$Q = \frac{T}{2}\frac{\Delta i_L}{2}\frac{1}{2} = \frac{3\mu s}{2}\frac{1.25}{2}\frac{1}{2} = 4.6875 * 10^{-7} C \tag{4.4}$$

An ideal capacitor is wholly characterized by a constant capacitance *C*, defined as the ratio of charge *Q* on each conductor to the voltage *V* between them:

$$C = \frac{Q}{V} \tag{4.5}$$

As it was said before the capacitor is a nonideal component, therefore we will take into account an ESR which increases the voltage across the branch. Since we do not know yet the value of that resistance we consider that the whole voltage is a sum of the capacitor's voltage and the resistance's one.

$$\Delta V_0 = \Delta V_C + \Delta V_{RC} \tag{4.6}$$

Firstly we will use just the 50% of ΔV_0 to calculate C:

$$C = \frac{Q}{\Delta V_C} = \frac{4.6875 * 10^{-7}}{5 * 0.01 * 0.5} = 18.75\mu F$$

Checking the different types of capacitors, the most similar is a Wet Tantalum Capacitor with a 20 μF capacitance with an equivalent series resistance of 1.99 Ω.

The next step will be to check how big ESR we can tolerate. The ripple current should pass the ESR.

Then

$$1.25\ \mathrm{A} * \mathrm{ESR} = 0.5\% * 5\mathrm{V}$$

giving an ESR=0.02 Ω

As we can see the tantalum capacito does not fulfill this. Then we try to find a ceramic capacitor instead.

In these conditions we will use a surface mount multiplayer ceramic chip capacitor with $68\ \mu F$ capacitance. In the datasheet the ESR is given as a dissipation factor.

$$DF = ESR * \omega * C \quad (4.7)$$

Where,

$$\omega = 2\pi * f_{SW} \quad (4.8)$$

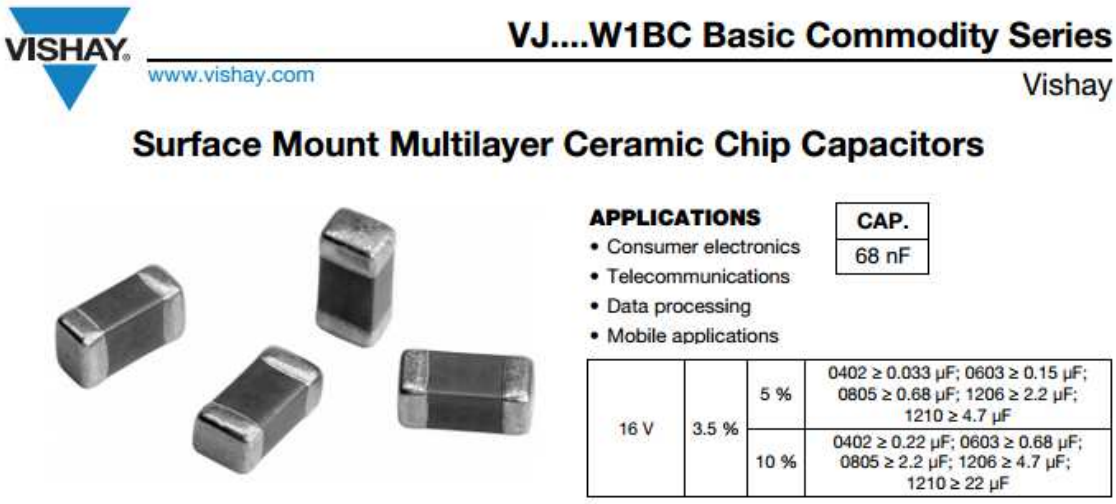

VISHAY
www.vishay.com
VJ....W1BC Basic Commodity Series
Vishay
Surface Mount Multilayer Ceramic Chip Capacitors
APPLICATIONS
• Consumer electronics
• Telecommunications
• Data processing
• Mobile applications
CAP.
68 nF
16 V | 3.5 % | 5 % | 0402 ≥ 0.033 µF; 0603 ≥ 0.15 µF; 0805 ≥ 0.68 µF; 1206 ≥ 2.2 µF; 1210 ≥ 4.7 µF
16 V | 3.5 % | 10 % | 0402 ≥ 0.22 µF; 0603 ≥ 0.68 µF; 0805 ≥ 2.2 µF; 1206 ≥ 4.7 µF; 1210 ≥ 22 µF

Figure 16. Capacitor datasheet.

The ESR for this capacitor is:

$$ESR = \frac{DF}{\omega * C} = 0.025\Omega$$

Using a bigger capacitance will give a much smaller voltage ripple due to the capacitance value. It will be about:

$$\Delta \mathrm{V} = \frac{\mathrm{Q}}{\mathrm{C}} = \frac{5 * 10^{-7}}{60 * 10^{-6}} = 8 * 10^{-3} V$$

leaving the most ripple for the ESR. The ESR ripple will be:

$$1.25A * 0.025 = 0.03V$$

Then we fulfill the requirements.

4.3. Diode:

The diode losses represent an important percent of the total losses (Usually over 50%) [10]. So power dissipation is the limiting factor when choosing a diode. The power dissipated by a diode is:

$$P_D = V_D I_D \tag{4.9}$$

Where V_D is the voltage drop across the diode at the given output current. Typical values are 0.7 Volts for a silicon diode and 0.3 Volts for a Schottky diode. Own to this we will try to choose a Schottky diode whose switching losses are also negligible. As lower is the voltage drop, higher is the efficiency [5]. Besides, the diode's forward current specification must exceed the maximum output current and we must ensure that the reverse-repetitive maximum voltage is greater that the input voltage.

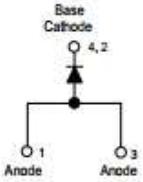
According to these conditions we choose a Schottky rectifier 50WQ10FNPbF whose forward voltage is 0.63 Volts at the current of 5 Amperes.

International
IOR Rectifier 50WQ10FNPbF

SCHOTTKY RECTIFIER 5.5 Amp

Characteristics	Values	Units
$I_{F(AV)}$ Rectangular waveform	5.5	A
V_{RRM}	100	V
I_{FSM} @tp=5µs sine	330	A
V_F @5 Apk, T_J=125°C	0.63	V
T_J range	-40 to 150	°C

Case Styles



D-PAK (TO-252AA)

Figure 17. Diode datasheet.

4.4. MOSFET:

Choosing the MOSFET is a complicated task because calculating power loss in a switching MOSFET is not as simple as it first seems [6].

On the one hand, the first cause of power loss in a MOSFET is the dissipation due to the intrinsic resistive element [7]. This dissipation only occurs when current is conducted through the device. This resistive parameter is called R_{DS}. Worth saying that these conduction losses are inversely proportional to the size of the MOSFET.

On the other hand, the second cause of power loss is due to switching losses [8]. It exists an intrinsic parasitic capacitance which stores and dissipates energy during the transition from OFF to ON state and the opposite. In this case, switching losses depend on the switching time and also the size of the MOSFET. The larger the size of the MOSFET and the switching time, the higher its switching losses.

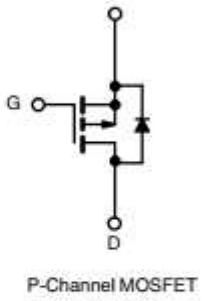
According to this, we will find the balance between these two aspects, in order to choose the most proper MOSFET.

VISHAY

SUD45P03-09

Vishay Siliconix

P-Channel 30 V (D-S) MOSFET



P-Channel MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 30	0.0087 at V_{GS} = - 10 V	- 45[d]	60
	0.0150 at V_{GS} = - 4.5 V	- 32	

Parameter	Symbol	Min.	Typ.	Max.	Unit
Turn-On Delay Time[c]	$t_{d(on)}$		12	20	ns
Rise Time[c]	t_r		11	14	
Turn-Off Delay Time[c]	$t_{d(off)}$		40	60	
Fall Time[c]	t_f		12	14	
Drain-Source On-State Resistance[a]	$R_{DS(on)}$		0.0072	0.0087	Ω
			0.0125	0.0150	

Figure 18. MOSFET datesheet.

5. Efficiency:

It is time to tackle the main target of this project: The efficiency calculation. To do it, we will calculate separately the different losses in each section of the converter. We know that the power dissipated by a resistance is:

$$P = I^2 R \tag{4.10}$$

5.1. Losses in the inductor:

The power dissipated due to the copper losses is:

$$P_I = I_0^2 * R_L = 25*8.3*10^{-3} = 0.2075W$$

Where I_{load} is the maximum current through the inductor.

5.2. Losses in the capacitor:

To satisfy the output voltage ripple condition, we chose a capacitor whose ESR is 0.77 Ohms. Besides, we were aware that choosing a capacitor with very low ESR may cause the power converter to be unstable[10].

The estimated power dissipation in the capacitor is:

$$P_C = I_{ripple}^2 * ESR = 1.25^2 * 0.025 = 0.039W$$

5.3. Losses in the diode:

As it was said before, the losses in the diode are over the 50% of the total losses. The diode's average current is equal to the output current times the portion of time the diode is conducting $(1 - D)$. The diode is conducting only when the source is disconnected, otherwise the source supplies the reverse voltage needed to avoid the conduction through the diode [10 and 12].

$$I_D = (1 - D)I_0$$

In these conditions, the worst case average power dissipated can be calculated as follows:

$$P_D = V_D I_D$$

In our case V_D is equal to 0.63 Volts. Now the power dissipation is:

$$P_D = V_D I_D = 0.5 * 5 * 0.63 = 1.575W$$

5.4. Losses in the MOSFET:

The next figure provides a rough estimate about the behavior of the MOSFET:

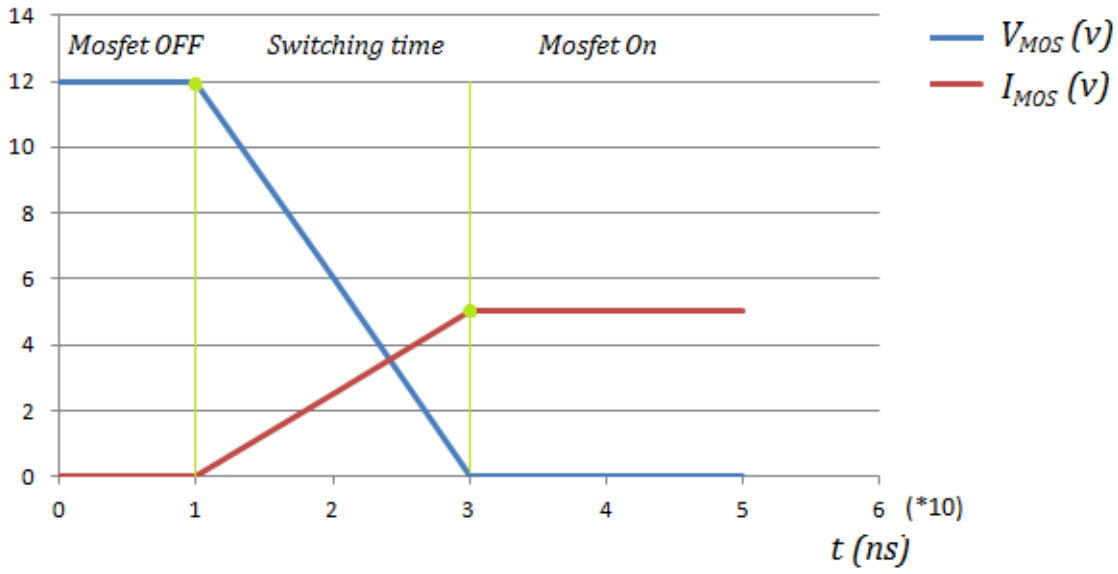


Figure 19.MOSFET behavior.

As we can see, there are the two different types of losses in the MOSFET [11].

5.4.1. Conduction Losses:

The MOSFET's average current is equal to the output current times the portion of time the MOSFET is conducting (D). The diode is conducting only when the source is connected.

So:

$$P_{conduction} = (I_0 D)^2 R_{DS} = 2.5^2 * 0.0087 = 0.0544W$$

5.4.2. Switching Losses:

According to figure, the variation of the voltage and the current has been considered as a line. In these conditions, the general expression for power dissipation during the switching time is:

$$P_{SW}(t) = \int i(t)v(t)dt * f_{SW} = \int_0^t (At + B)(Ct + D)dt = \int_0^t (ACt^2 + ADt + BCt + BD)dt = |\frac{ACt^3}{3}|+|\frac{ADt^2}{2}|+|\frac{BCt^2}{2}|+|\text{BDt}|= (|\frac{ACt^3}{3}|+|\frac{(AD+BC)t^2}{2}|+|\text{BDt}|)* f_{SW} \quad (4.11)$$

Where $(At + B)$ is the equation of the current through the MOSFET during the switching time, $(Ct + D)$ the equation for the voltage across the MOSFET during the switching time and f_{SW} the switching frequency. The top integral limit is the time. It means the time between the OFF state and the ON state.

For the chosen MOSFET the rise time is equal to the fall time and the equations which describe the behavior of the voltage and the current are:

$$v(t) = (Ct + D) = -6 * 10^8 x + 12$$
$$i(t) = (At + B) = 2.5 * 10^8 x$$

In each period the power dissipated is:

$$P_{SW}(t) = (|\frac{ACt^3}{3}|+|\frac{(AD+BC)t^2}{2}|+|\text{BDt}|)* f_{SW} = 0.1333W$$

For the rise time and the fall time:

$$P_{SW}(t) = 2 * 0.1333 = 0.2666W$$

5.5. Efficiency Calculation:

The output power is the output voltage times the output current [12].

$$P_0 = V_0 * I_0 = 25W$$

$$P_I = 0.2075\text{W}$$

$$P_C = 0.039W$$

$$P_D = 1.575W$$

$$P_{conduction} = 0.0544W$$

$$P_{SW} = 0.2666W$$

$$P_{Buck} = P_I + P_C + P_D + P_{SW} + P_{conduction} = 2.0881W$$

$$Efficiency \equiv \eta = \frac{P_0}{P_0 + P_{Buck}} = 0.92106 \qquad (4.12)$$

$$\eta = 92.106\%$$

6. Simulation.

At first, the mathematical system model was obtained, then components were chosen and their losses were calculated. Now, it is time to simulate their behaviour in the circuit. To simulate it, we introduce the values of the components and the matrixes in Matlab R2012. After the first simulation, other three different experiments will be made in order to evaluate possible changes in the efficiency.

6.1 Simulation of the system.

The model in Simulink is developed as below.

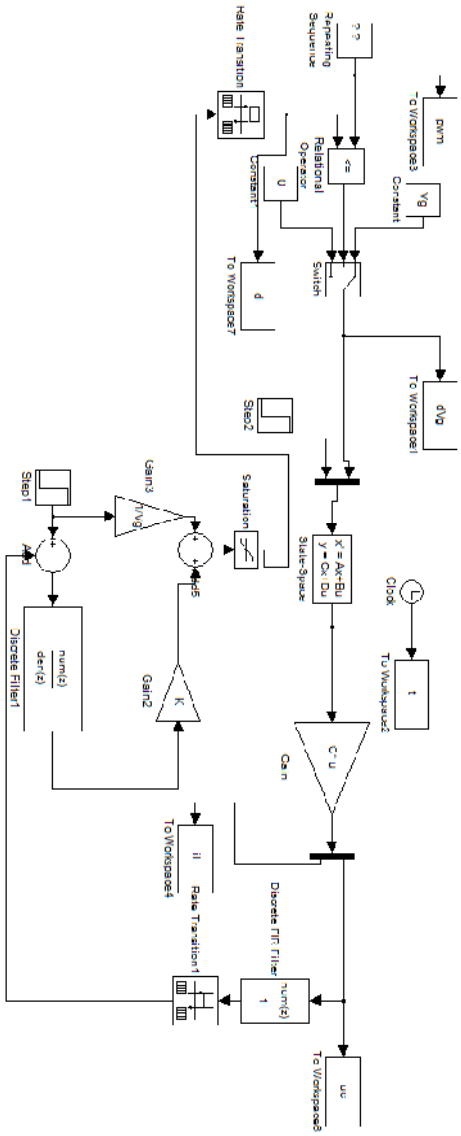


Figure 20. Model in simulink.

In the first part of the model, we can observe how the signal provided by the PWM is compared to the feedback signal. From that comparison the voltage source might be connected to the system.

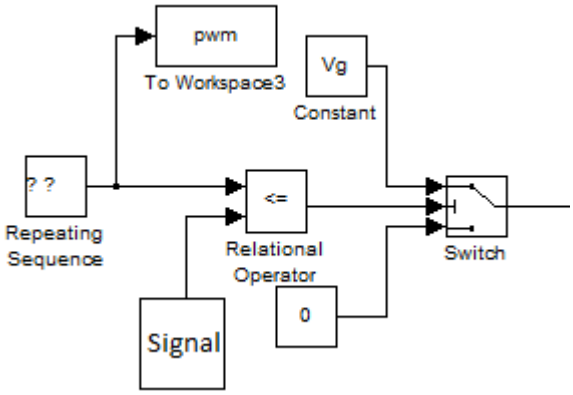


Figure 21. Comparison block.

The blocks on the right tell about the matrixes which describe and control the behavior of the system. The matrix block receives the voltage source as input. Finally, the outputs can be observed: the inductor current and the capacitor voltage.

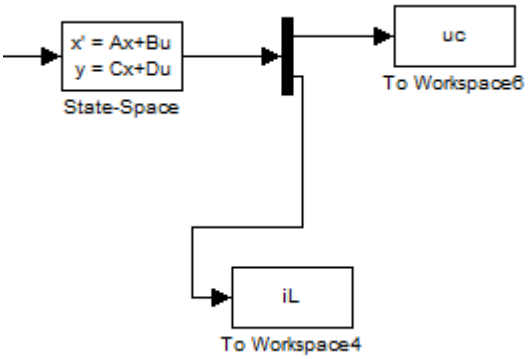


Figure 22. Matrix and output blocks.

The rest of the blocks refer to the feedback system, where the output voltage is compared to the reference voltage.

The simulation shows the results. In the figure below it is possible to see how the voltage source is connected when the feedback signal is bigger than the PWM signal.

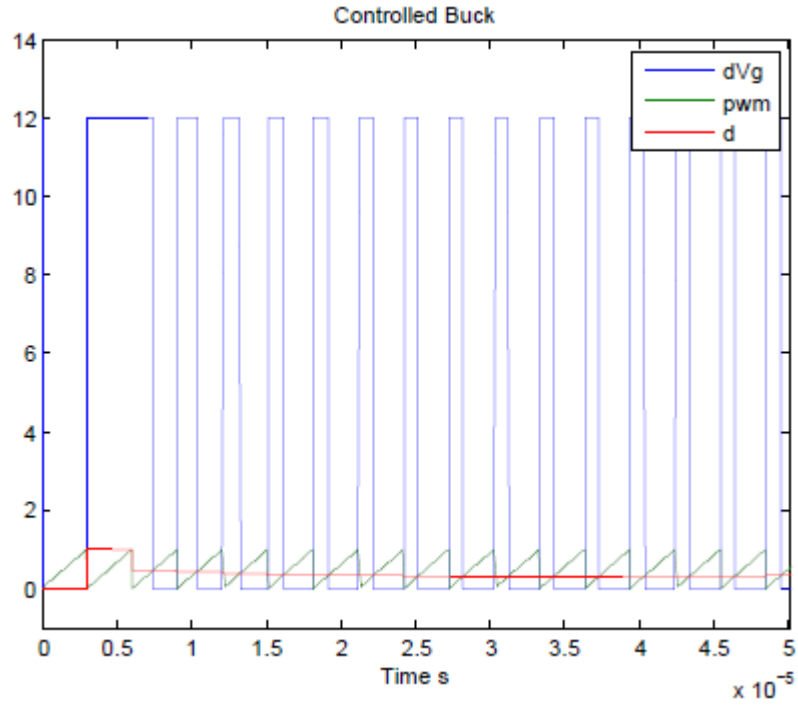


Figure 23. Voltage, PMW and duty cycle signals. Units on y-axis are from 0 to 14. Units on x-axis are from 0 to 50µs

Also, it is possible to observe the outputs. In the first case, the inductor current ripple must be lower than 25% and secondly the output voltage ripple lower than 1%. As we can see, these two requirements are satisfied.

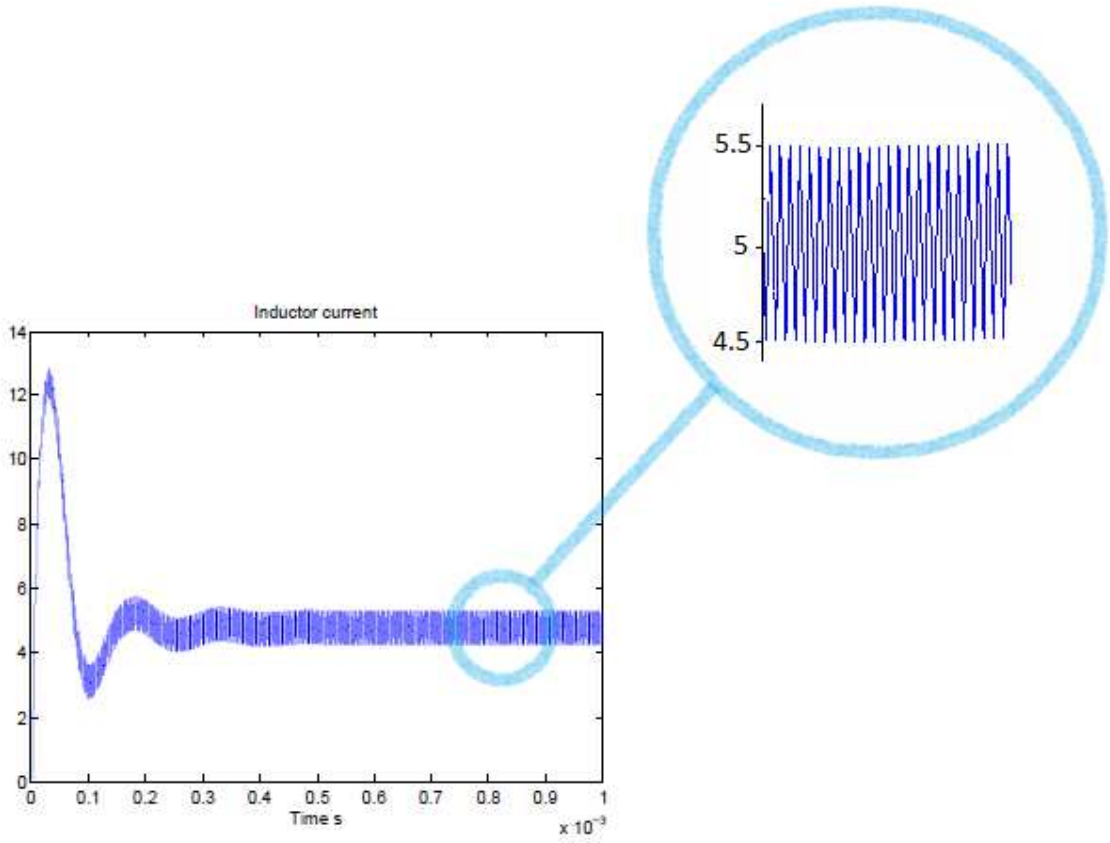


Figure 24. Inductor current and inductor current ripple. Units on y-axis are from 0 to 14 Amperes. Units on x-axis are from 0 to 1ms.

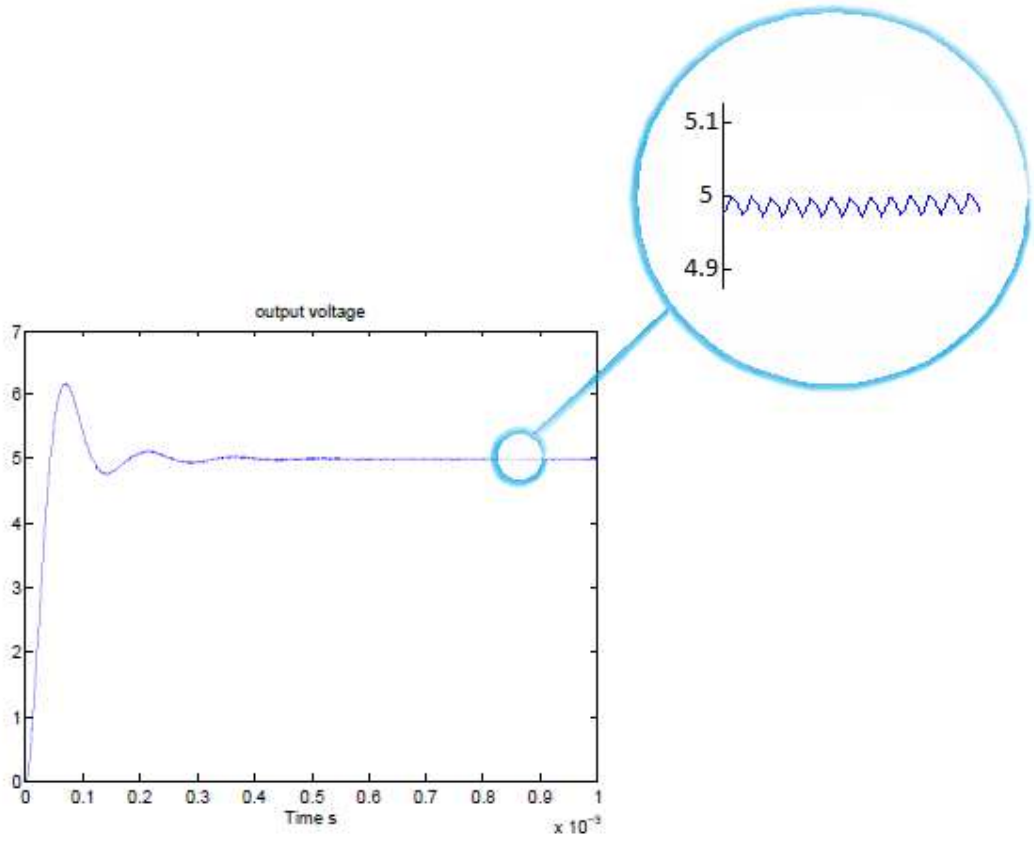


Figure 25. Output voltage and output voltage ripple. Units on y-axis are from 0 to 7 Volts. Units on x-axis are from 0 to 1ms.

The simulation also gives us the possibility of analyzing the conduction losses. A simple I^2R power dissipation equation can be used, except on the diode. These losses depend on the inductor current. Therefore, their graphs have the same behavior as the inductor current.

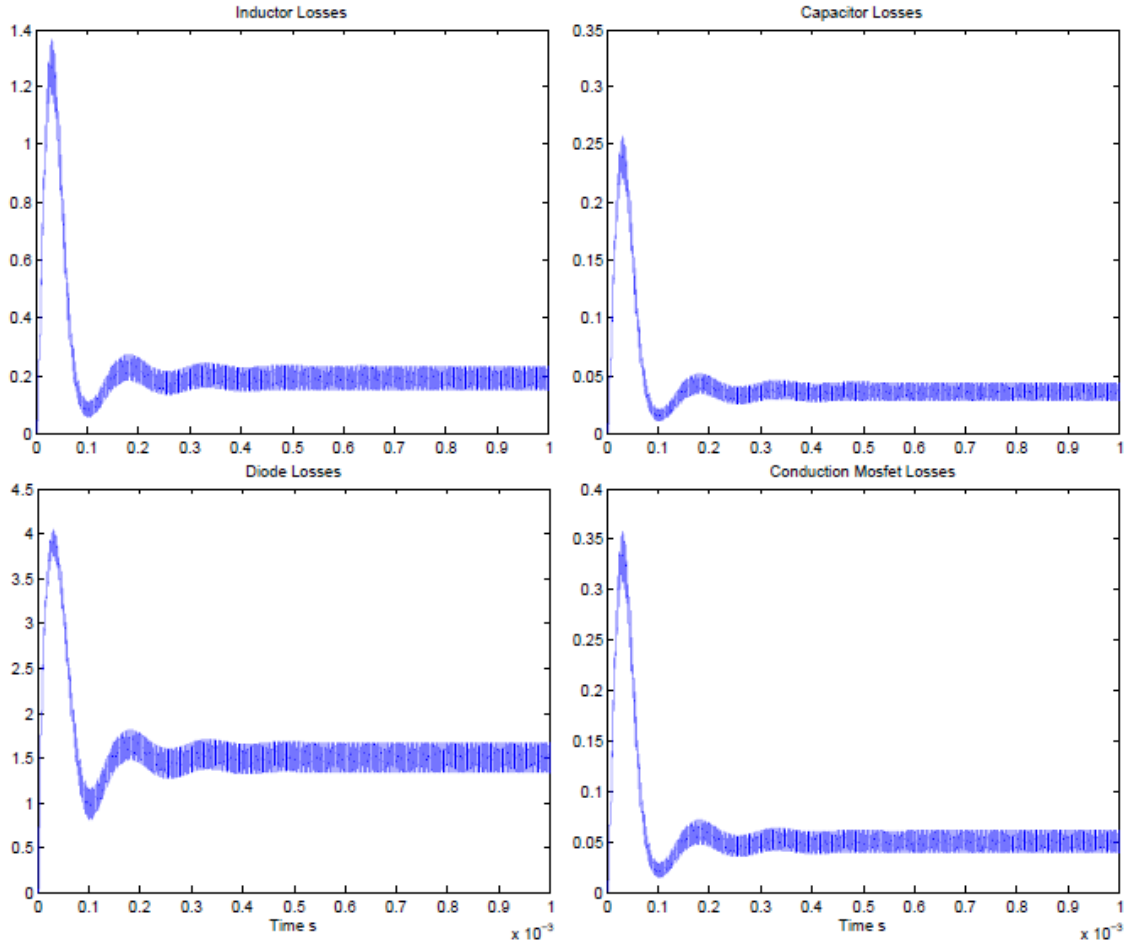


Figure 26. Conduction power losses. Units on y-axis are: In 26.1 from 0 to 1.4 Watts. In 26.2, from 0 to 0.35 Watts. In 26.3, from 0 to 4.5 Watts and in 26.4, from 0 to 0.4 Watts. Units on x-axis are from 0 to 50µs.

The efficiency given by the simulation is 91.00% and the percent of power loss consumed by each component is shown in the figure below.

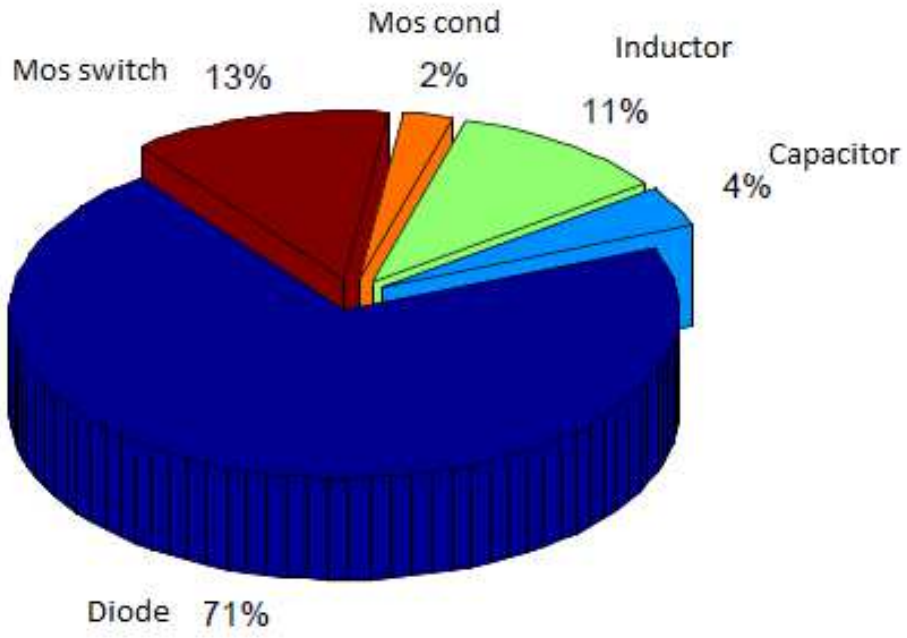


Figure 27. Power losses pie chart.

6.1.1. Conclusions of the simulation:

The previous simulation provided us an estimated behavior of the system. Worth saying that power loss dissipated by the diode is quite elevated despite being a Schottky type. This problem could be solved replacing the diode by another mosfet, but in this case we did not need it because power consumed by the rest of the components is so reduced that the efficiency was over 90%.

6.2 Experiment to determinate the highest efficiency:

In this paragraph, some changes in the previous specifications will be made in order to achieve the optimal conditions to reach the highest possible efficiency of the system.

At first, the output current will be changed within a ratio from 0 to 5 Amperes keeping constant the output voltage to 5 Volts. Consequently, that change causes variations in the load which will be also analyzed.

Then, we will repeat the experiment but in this case firstly the output voltage will be set to 9 and secondly to 1 Volts.

6.2.1 First experiment:

Specifications:

$$V_0 = 5V$$
$$V_{NOM} = 5V$$
$$V_{IN} = 12V$$
$$\Delta I \leq 25\%$$
$$\Delta V_0 = 1\%$$
$$0 \leq I_0 \leq 5A$$

The last condition implies that each case will be analyzed separately from 0 to 5, testing the efficiency for each different current value.

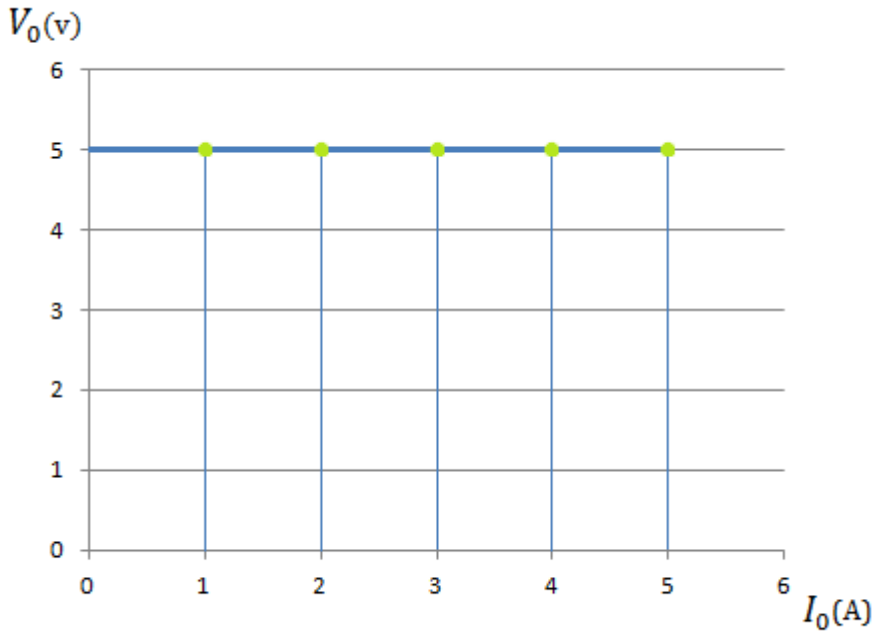


Figure 28. First experiment. Variation of the output current.

To get different output current values, the load is changed from 1 to 5 Ohms and the efficiency in each case is:

V_0	I_0	R	ΔI_0	η
5	5	1	0,05	91
5	4	1,25	0,04	91,02
5	3	1,666	0,03	90,92
5	2	2,5	0,02	90,48
5	1	5	0,01	88,7
5	0	inf	0	X

Table 1. First experiment table.

The ratio between the output current and the efficiency is shown in the next graph:

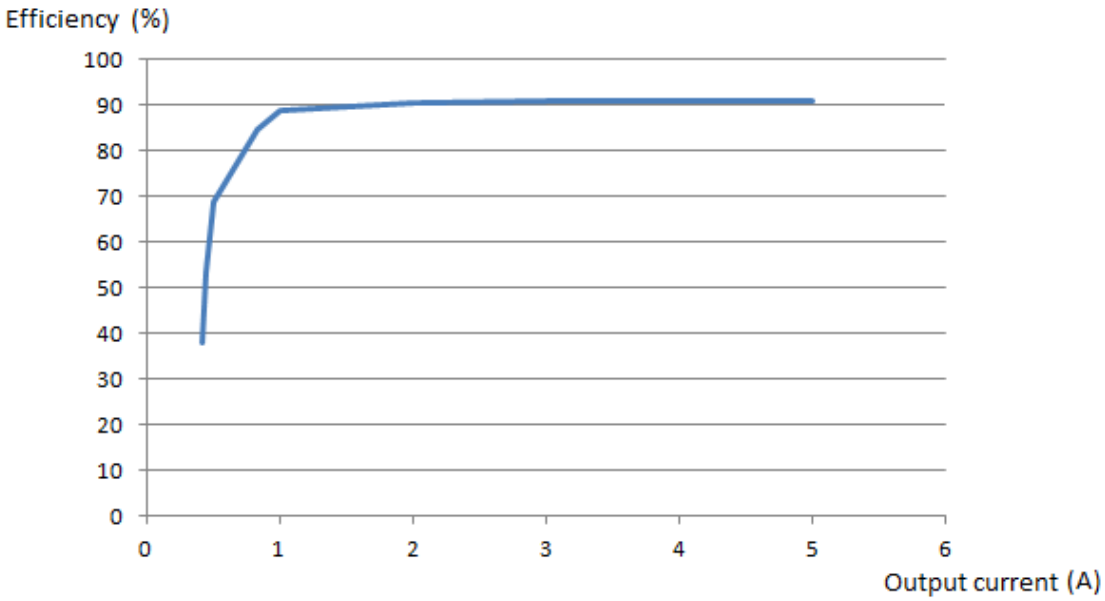


Figure 29. Ratio between efficiency and output current.

As we can see, within the interval from 1 and 0 Ampere the efficiency decreases rapidly, being lower than 40% when the output is 0,5 Amperes.

6.2.2. Second Experiment:

In this case we set the output voltage to 1 Volt and simulate several times, changing the value of the output current from 0 to 5 Amperes.

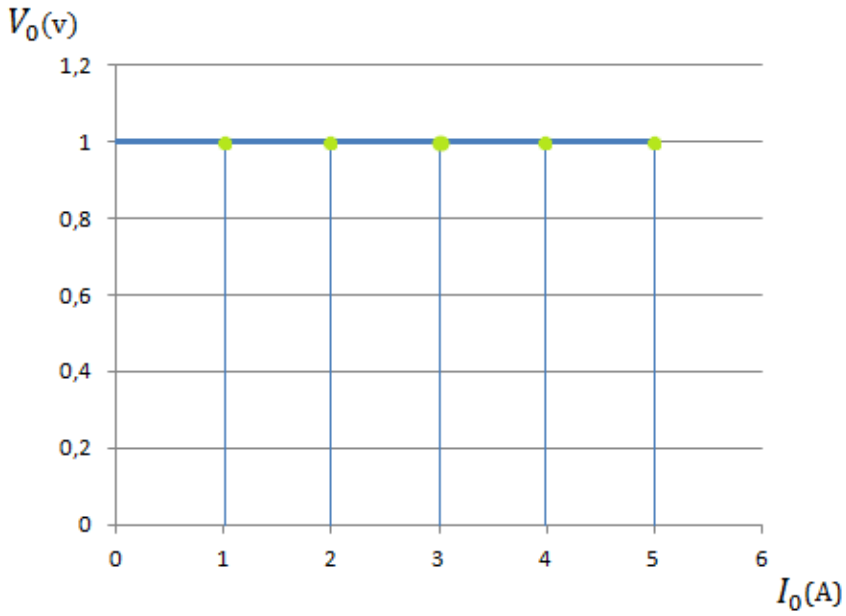


Figure 30. Second experiment. Variation of the output current.

According to these specifications, the values of the load are calculated and tested in the simulation. The efficiency results are:

V_0	I_0	R	ΔI_0	η
1	5	0,2	0,05	59,77
1	4	0,25	0,04	60,81
1	3	0,333	0,03	61,81
1	2	0,501	0,02	62,74
1	1	1	0,01	63,37
1	0	inf	0	X

Table 2. Second experiment table.

In this second experiment the voltage is set to 1 Volt. In these conditions the maximum efficiency is only 63,37% and in this case it is higher when the output current is lower.

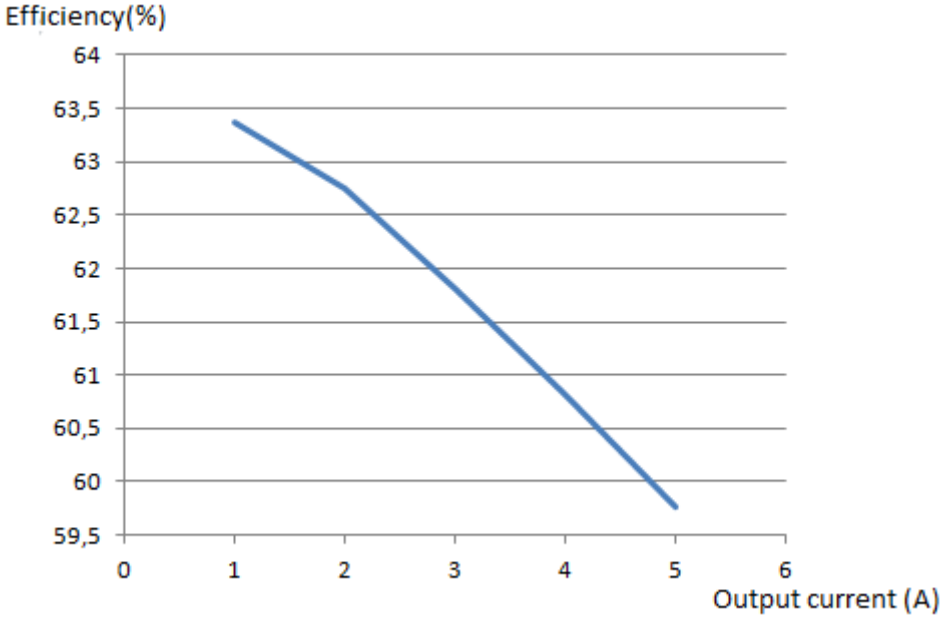


Figure 31. Ratio between efficiency and output current.

6.2.3 Third experiment:

For the last experiment, the output voltage is equal to 9 Volts and we proceed to simulate for the different cases, changing the output current from 0 to 5 Amperes.

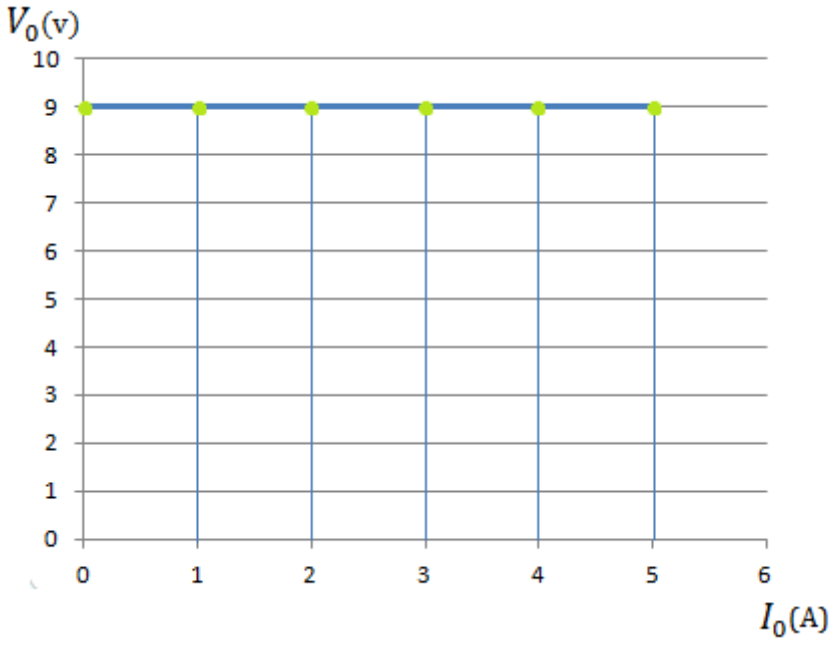


Figure 32. Third experiment. Variation of the output current.

Using the last value of V_0 to calculate R, the results obtained are shown next:

V_0	I_0	R	ΔI_0	η
9	5	1,8	0,05	94,26
9	4	2,25	0,04	94,06
9	3	3	0,03	93,62
9	2	4,5	0,02	92,65
9	1	9	0,01	89,45
9	0	inf	0	X

Table 3. Third experiment table.

In this case, the output voltage is set to 9 Volts and the efficiency increases until 94%.

The ratio between the efficiency and output current is shown in the next graph:

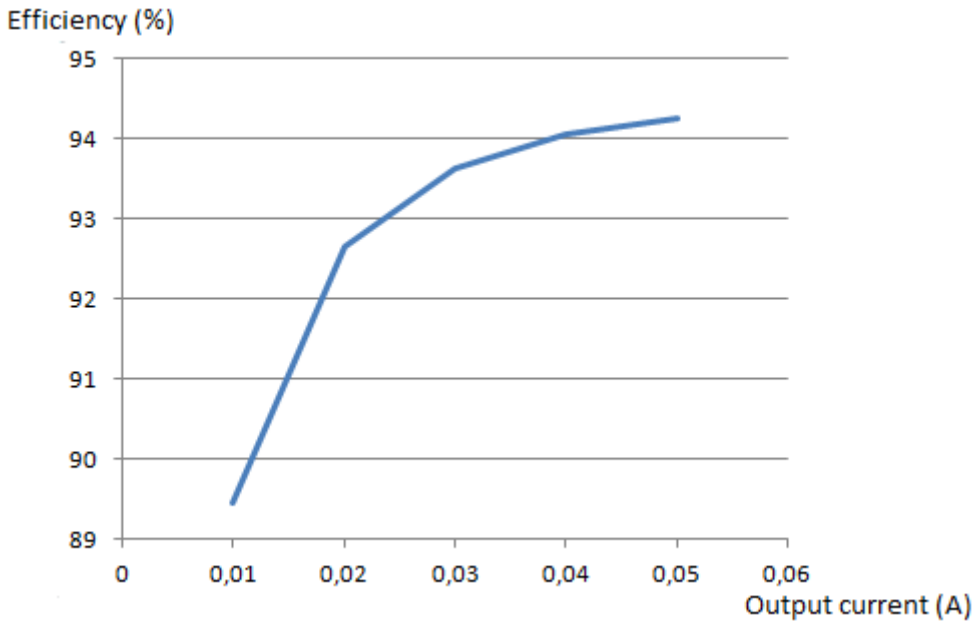


Figure 33. Ratio between efficiency and output current.

6.2.4. Conclusions from the experiments:

From the previous experiments it is possible to observe that the smaller the difference between the input voltage and the output voltage, the higher the efficiency of the system. Besides, when the output voltage is enough to reach a high efficiency, there is a direct proportion between the output current and the efficiency.

7. Conclusion.

This thesis work describes which methods were used to choose the most proper components in order to reach the highest possible efficiency of a Buck Converter. Besides, other suggestions were given to improve even more the efficiency. Firstly, the system was described using space state equations which could be useful to simulate the behaviour of the system. Real components were proposed, attaching also their datasheet and identifying the most important parameters. Secondly, a simulink model of a buck converter was designed and used to simulate the system. After that, we had to replace the tantalum capacitor by a ceramic capacitor with lower ESR in order to reduce the output voltage ripple. Hence, this thesis can be useful to find real components to design an efficient Buck Converter.

8. References.

[1] Issa Batarshe, “Power Electronic Circuits”. John Wiley Publisher, 2003.

[4] Karlsson, M. R&D Power Modules, Ericsson AB, Kalmar, Sweden, Holmberg, T. Lenells,M. “Analysis of a capacitive loaded buck converter” Digital Object Identifier: 10.1109/INTLEC.2009.5351804, Telecommunications Energy Conference, 2009. INTELEC 2009. 31st International

[5] Kenneth A. Kuhn, “Diode Specifications”, 1 Sept. , 2008, pp. 1-2.

[6] Jess Brown, “Document Number: 73217 - Power MOSFET Basics: Understanding Gate Charge and Using It To Assess Switching Performance”, 2 December 2008, pp.3.

[7] Jess Brown Guy Moxey, “Document Number: 71933, Power MOSFET Basics: Understanding MOSFET Characteristics Associated With The Figure of Merit”, 8 September 2003, pp.3.

[8] Mohan, Underland and Robbins. “Power Electronics, converters, Applications and Design,” ISBN 0-471-58404-8

[9] Arnoldo Pacheco Alamos, “Análisis de Pérdidas del Convertidor Buck Síncrono para Aplicaciones Móviles” 20 April 2007, pp. 13-23

[10] Donald Schelle and Jorge Castorena, “Buck-Converter Design Demystified”, in Donald Schelle and Jorge Castorena, Power electronics technology, June 2006, pp. 46-52.

[11] Andrew Smith, “Calculating power loss in switching MOSFETs”, 31 July 2011.

[12] Volkan Kursun, Siva G. Narendra, Vivek K. and Eby G. Friedman “Efficiency Analysis of a High Frequency Buck Converter for On-Chip Integration with a Dual-VDD Microprocessor”, ESSCIRC 2002.

[13] Shun Yang, “Modelling and control of a Buck converter” 22 June 2011. pp.11-22

[14] Madhu Kiran & Partha Saradhi, “Control of Buck converter by polynomial PID and PD controllers” June 2012. pp.7-10.

9. Appendix.

9.1. Matlab code.

```
%%
%% BMR450 Simple controller

%% Circuit data
%BMR power train data
Lb=8.4e-6;
Cb=86e-6;
R=1;
Rl=8.3e-3;
Rc=0.77;
% extra capacitor load
Cb2=300e-6;
% input voltage
Vg=12;
% load current parameters
T_I0_step=0.5e-3;
I0_initial=0;
I0_final=5;
%pwm signal frequency
fs=330e3;
%Samplinginterval for the pwm generator
% 100 samples per pwm period time
hpwm=1/fs/100;
%Set point, desired output voltage
yRef=5;


%Sampling interval for the controller
%should be >= 1/fs
h=1/fs;

%Model
A=[-(Rl+(R*Rc/R+Rc))/Lb,-(R/R+Rc)/Lb;(R/(R+Rc))/Cb,-
(1/R+Rc)/Cb];
%Input signals duty cycle and load current
B=[1/Lb,0;0,0];

%output signals, the two states
C=[(R*Rc)/(R+Rc),R/(R+Rc);Rc/(R+Rc),1/(R+Rc)];
```

```
D=[0,0;0,0];
%Initial values
%capacitor voltage
uC0=0;
%inductor current
iL0=0;

%% Code for controller part

%Continuous system
%State space model
Gpss=ss(A,B(:,1),C(1,:),D(1,1));
%Transfer function model
Gptf=tf(Gpss);

%Discrete system
%Transfer function
Gpdtf=c2d(Gptf,h,'zoh');

%B polynom and A polynom
[Btf,Atf]=tfdata(Gpdtf,'v');
%polynom coefficients
b1=Btf(2);
b2=Btf(3);
a1=Atf(2);
a2=Atf(3);


%Control parameters in BMR450, design open system
%frequency resonance peak
wp=1/sqrt(Lb*Cb);

%Introduce a derivative link for stabilization (1 + Td*s)
%Introduce the derivative at a frequency slightly below of
the resonance peak
Td1=1/wp*4;

% Implement the derivative as a differance ratio (1 + Td*(1
- z^-1)/h
%=proportional to(1 + Td/(Td+h)*z^-1)

zp1=Td1/(h+Td1);

Td2=1/wp*4;

zp2=Td2/(h+Td2);

%numerator in case of integral action
%dpoly=conv([1 -zp1],[1 -zp2]);

%numerator in case of no integral action
```

```
dpoly=[1 -zp1];


%integral action and control delay
%cpoly=[1 -1 0];

%no integral action
cpoly=1;

%design of gain
K=32e-2;

%Discrete controller
R2=tf(K*dpoly,cpoly,h);
%Discrete closed system
Md2=feedback(Gpdtf,R2);
eigMd2=eig(Md2);
abseigMd2=abs(eigMd2)

%% Simulation

%Simulation
[T,X,Y]=sim('prueba2',1e-3);

%plot
figure(11)
plot(t,dVg/8,t,pwm,t,uc,t,d)
legend('dVg','pwm','uc','d')
title('Controlled Buck')
xlabel('Time t')
axis([0 1e-3 0 15])

figure(12)
plot(t,dVg/8,t,pwm,t,uc,t,d,t,iL)
legend('dVg','pwm','uc','d','iL')
title('Controlled Buck')
xlabel('Time t')
axis([0 1e-3 0 15])

figure(13)
plot(t,uc)
axis([0 0.2e-2 0 10])

figure(11)
plot(t,dVg,t,pwm,t,uc,t,d)
legend('dVg','pwm','uc','d')
title('Controlled Buck')
xlabel('Time t')

figure(12)
plot(t,iL)
```

```
legend('iL')
title('Controlled Buck')
xlabel('Time t')

figure(13)
plot(t,pwm)
legend('PWM')
axis([0 1.5e-3 0 1 ])

figure(14)
plot(t,dVg)
legend('dVg')
axis([0 1.5e-3 -2 15])

figure(15)
plot(t,uc)
legend('uc')
axis([0 1.5e-3 0 3])

figure(16)
plot(t,d)
legend('d')
axis([0 1.5e-3 0 2])

figure(11)
plot(t,dVg/8,t,pwm,t,uc)
xlabel('Time t')
legend('dVg/8','PWM','uc')
axis([0 1.5e-3 -0.5 15])
```

9.2. Simulink blocks.

Simulink blocks pictures are shown in chapter 6.